

This listing of claims will replace all prior versions,  
and listings, of claims in the application:

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Q' 1 Claim 1 (currently amended): A method of decoding  
2 encoded image data comprising the steps of:  
3           operating a decoder circuit implemented in  
4 hardware to perform at least one non-memory intensive  
5 image decoding operation to generate, from the encoded  
6 image data, a first set of processed image data, the at  
7 least one non-memory intensive image decoding operation  
8 ~~being an operation in the group of operations consisting~~  
9 ~~of a variable length decoding operation, an inverse scan~~  
10 ~~conversion operation, and an inverse quantization~~  
11 ~~operation;~~  
12           supplying the first set of processed image data  
13 generated by the decoder circuit to a programmable  
14 processor; and  
15           operating the programmable processor to perform  
16 at least one additional image decoding operation using  
17 the first set of processed image data.

1 Claim 2 (original): The method of claim 1, wherein the  
2 step of operating the decoder circuit, includes the step  
3 of performing at least two additional operations from the  
4 group of operations consisting of a variable length  
5 decoding operation, an inverse scan conversion operation,  
6 an inverse quantization operation, an inverse discrete  
7 cosine transform operation, and a data reduction  
8 operation, the two additional operations being different  
9 from said at least one non-memory intensive operation.

1 Claim 3 (original): The method of claim 1, wherein the  
2 step of operating the decoder circuit further includes:  
3 operating the decoder circuit to perform a data reduction  
4 operation.

1 Claim 4 (currently amended): ~~The method of claim 2, A~~  
2 method of decoding encoded image data comprising the  
3 steps of:

4 operating a decoder circuit implemented in  
5 hardware to perform at least one non-memory intensive  
6 image decoding operation to generate, from the encoded  
7 image data, a first set of processed image data, the at  
8 least one non-memory intensive image decoding operation  
9 being a variable length decoding operation;

10 supplying the first set of processed image data  
11 generated by the decoder circuit to a programmable  
12 processor;

13 operating the programmable processor to perform  
14 at least one additional image decoding operation using  
15 the first set of processed image data; and

16 wherein the step of operating the decoder circuit  
17 further includes:

18 operating the decoder circuit to perform a data  
19 reduction operation.

1 Claim 5 (original): The method of claim 2, wherein the  
2 step of operating the programmable processor to perform  
3 at least one additional image decoding operation includes  
4 the step of:

5       operating the programmable processor to perform a  
6 motion compensated prediction operation.

1 Claim 6 (original): The method of claim 5, wherein the  
2 step of operating the programmable processor to perform  
3 at least one additional image decoding operation further  
4 includes the step of:

5       operating the programmable processor to combine  
6 decoded image data produced by performing the motion  
7 compensated prediction operation with decoded residual  
8 image data to produce a set of decoded image data  
9 representing reconstructed pixels.

1 Claim 7 (original): The method of claim 1, wherein the  
2 step of operating the programmable processor to perform  
3 at least one additional image decoding operation includes  
4 the step of:

5       operating the programmable processor to combine  
6 decoded image data produced by performing a motion  
7 compensated prediction operation with decoded intra-coded  
8 image data to produce a set of decoded image data  
9 representing a complete frame.

1 Claim 8 (original): The method of claim 2, wherein the  
2 programmable processor is coupled to a graphics  
3 processor, the method further comprising the step of:  
4 operating the graphics processor to perform a motion  
5 compensated prediction operation using data included in  
6 the first set of processed data.

1 Claim 9 (original): The method of claim 8, wherein the  
2 step of operating the programmable processor to perform  
3 at least one additional image decoding operation further  
4 includes the step of:

5 operating the programmable processor to combine  
6 decoded image data produced by performing the motion  
7 compensated prediction operation with decoded residual  
8 image data to produce a set of decoded image data  
9 representing reconstructed pixels.

1 Claim 10 (currently amended): The method of claim 8,  
2 further comprising the step of:

3 storing in the decoder circuit multiple sets of  
4 context information for different video streams at the  
5 same time, each set of stored context information  
6 corresponding to a different one of a plurality of  
7 encoded video data streams processed by the decoder  
8 circuit each set of context information including  
9 vertical size, horizontal size and frame rate  
10 information.

1 Claim 11 (original): The method of claim 1, further  
2 comprising the step of:

3 storing in the decoder circuit multiple sets of  
4 context information, each set of stored context  
5 information corresponding to a different one of a  
6 plurality of encoded data streams processed by the  
7 decoder circuit.

1 Claim 12 (original): The method of claim 11, further  
2 comprising the step of:  
3           operating the decoder circuit to access the  
4 stored set of context information corresponding to an  
5 encoded data stream when the data stream is to be  
6 processed by the decoder circuit.

1 Claim 13 (original): The method of claim 12, wherein  
2 each set of stored context information includes encoded  
3 data stream syntax information.

Claims 14-18 (canceled)

1 Claim 19 (original): A method of decoding encoded image  
2 data comprising the steps of:  
3           operating a decoder circuit implemented in  
4 hardware to perform non-memory intensive image decoding  
5 operations to generate, from the encoded image data, a  
6 first set of processed image data, at least one of said  
7 non-memory intensive image decoding operation being a  
8 data reduction operation;  
9           supplying the first set of processed image data  
10 generated by the decoder circuit to a programmable  
11 processor; and  
12           operating the programmable processor to perform  
13 at least one additional image decoding operation using  
14 the first set of processed image data.

Claims 20-30 (canceled)